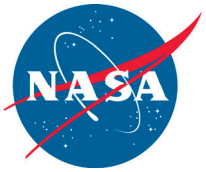
National Aeronautics and Space Administration



Interim Test Status Report for NEPP Scaled CMOS

Jessica N. Bowles-Martinez
Steven M. Guertin

Jet Propulsion Laboratory
Pasadena, California

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL Publication 10-13 10/10

National Aeronautics and Space Administration

Interim Test Status Report for NEPP Scaled CMOS

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

Jessica N. Bowles-Martinez
Steven M. Guertin

Jet Propulsion Laboratory
Pasadena, California

NASA WBS: 724297.40.49.11
JPL Project Number: 103982
Task Number: 03.02.02

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

http://nepp.nasa.gov

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

TABLE OF CONTENTS

ABSTRACT

This document reports the status of the NASA Electronic Parts and Packaging (NEPP) Scaled Complementary Metal Oxide Semiconductor (CMOS) Reliability effort for FY2010. This year's work concentrated on the development of a reliability test apparatus for DDR2 SDRAM devices and collection of initial data. This is an interim status report for this effort.

Preliminary test data on 78 nm 2 Gb DDR2 SDRAMs are presented as part of an ongoing effort to research mechanisms for reliability and physics of failure as part of the NEPP Scaled CMOS Reliability task

A commercial field programmable gate array (FPGA) board based test system capable of parallel operation of up to 9 devices was developed to collect device-under-test (DUT) data. This system collects parametric data correlated with operating mode and data retention characteristics of the storage cells. This system has been used to collect preliminary data on devices at elevated voltage and elevated temperature.

1.0 CONTEXT AND INTRODUCTION

This report builds upon previous work conducted as part of the Scaled Complementary Metal Oxide Semiconductor (CMOS) Reliability task [1]. That task refines the understanding of device scaling and its impact on reliability through experimental data generated from tests performed on scaled DDR1 SDRAM devices and comparisons to known reliability models. That information was presented in the form of a user's guide, which was submitted to the NASA Electronic Parts and Packaging (NEPP) program.

This document serves as an interim report outlining work toward an updated user's guide. It describes a test system developed to gather data on updated and more highly scaled devices, the test matrix, and analysis of preliminary data. The test system exercises DDR2 SDRAM and can be used for testing in a variety of temperature and radiation environments. The data collected from tests in these environments will expand the user's guide to establish an approach for analyzing the reliability impact of space environments on real applications where devices are exposed to both temperature fluctuations and radiation.

The reported work concentrates on testing of commercial DDR2 devices using a test system developed at the Jet Propulsion Laboratory (JPL) to enable environmental stress under nominal operating conditions similar to those that would be seen in an application circuit. The test system is also used to establish device characteristics under a predefined set of operations. The tested characteristics were chosen based on the defined operating modes in the device specifications and based on known characteristics of arrays of DDR2 memory storage cells. The information collected, including operating current, cell-level retention time, and environmental stress history, will constitute the data used in the future during analysis of various failure mechanisms.

2.0 PARTS SELECTION

2.1 Part Type Selection Criteria

Memory devices with their high density of transistors, memory cells, and repetitive layout of memory blocks make them strong choices for experiments in reliability [1]. The appeal of SDRAM is in its prevalence in new popular technologies such as PCs, audio players, and digital cameras, as well as in upcoming flight projects. As a result, it is a key technology driver that is likely to respond to industry pressure with increased densities.

At the time of the previous data gathering, the DDR1 SDRAM was used as it was the industry standard and the most likely technology to be used for space applications. With the addition of DDR2 and DDR3, its use has been eclipsed by these upgraded technologies.

In order to provide the most relevant data for space applications, DDR2 SDRAM is the device type selected for test as DDR3 has not yet been considered for upcoming flight designs and DDR1 does not have the data rate needed for current applications. Based on current production rates and DRAM trend data [1], there should be a large supply and use of DDR2 parts for the next four years.

2.2 Selected Parts

In selecting DDR2 SDRAM devices for this test, it was necessary to locate parts that were 1 GB or greater, immediately in stock, available in a large quantity for statistically significant results (preferably with similar part lots), and represent a technology node smaller than previously tested DDR SDRAM. Both Samsung and Micron have 2 GB DDR2s, which meet the criteria for availability, timing, and technology node. Devices from both manufacturers were procured for this work. The details are given in Table 2.2-1.

The Samsung and Micron parts share similar internal organization and are both 78 nm technology devices. As a result, they fit a linear progression from previous tests [1] at technology nodes of 130 nm, 110 nm, and 90 nm.

These similarities are intended to ensure that tested parts from the two manufacturers are unlikely to have performance differences that stem from other, uncontrolled, factors. Therefore, relative performance can be more directly compared across devices from different manufacturers. The similar internal organization is also valuable in ensuring the portability of a test system to different parts with little or no changes to the tester design.

Table 2.2-1. Parts Tested

Manufacturer	2 GB Part Number	Size	Organization	Mounted Parts
Micron	MT47H256M8HG-**3:A**	78 nm	256Mx8	30
Samsung	K4T2G084QA-HC**F7**	78 nm	256Mx8	27

3.0 BOARD AND TEST SYSTEM DEVELOPMENT

3.1 Overview

Multiple approaches to test system development were investigated. The final approach of using a computer to control multiple test boards connected to device-under-test (DUT) boards was selected as the most appropriate, feasible, and robust solution for the long-term reliability tests.

3.2 Test Setup Options

Many test designs were considered, taking into consideration tester capabilities, test environments, resource availability, and manpower needed for implementation and conducting of tests. The following is a brief overview of test options considered with a focus on highlighting the hardware needed, available resources, and appropriateness for long-term stress testing.

3.2.1 Credence Tester and Multiplexer Test Board

This approach uses a Credence tester to send data to a DUT daughter board by multiplexing data through an intermediate test board. The Credence digital tester is a mixed signal and digital tester that sends data through a series of I/O pins that have custom test boards mounted on it. Signals from the Credence are sent to the DUT input/output (I/O) through 32-bit bursts that are multiplexed in the test board. The DUT receives 8-bits at a time after the 32-bits are multiplexed into four cycles. By doing this, the test board makes one 50 MHz cycle of data from the Credence function as four cycles of 8-bits to the DUT daughter boards, creating an effective data rate from the Credence of 200 MHz.

A system based on a single test board connected to the Credence has a lot of risk due to the high probability for damage when the DUTs are exposed to the temperature and radiation environments. The stresses may make the fairly high-cost test boards degrade and behave in a non-optimal way. If that occurs, it is difficult to decouple reliability issues on the test board from reliability issues in DUTs, making results inconclusive.

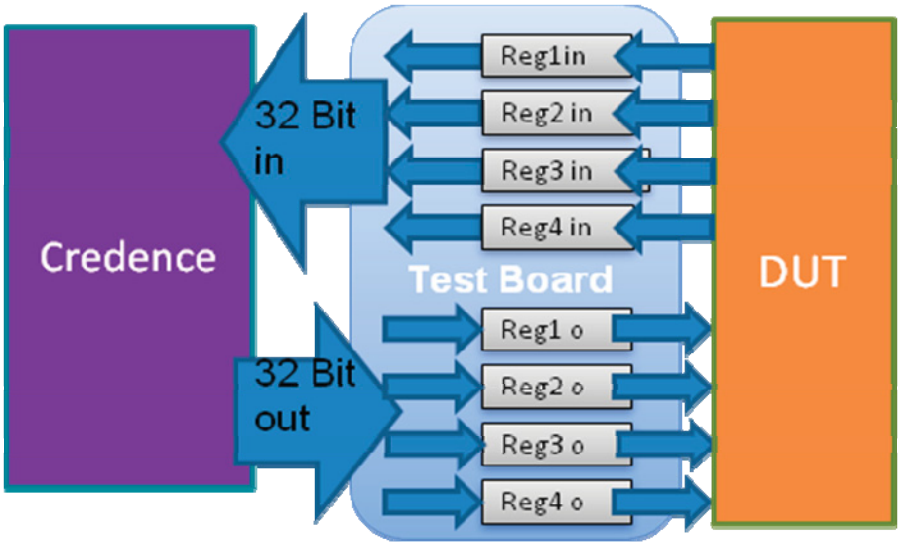


Figure 3.2-1. Credence-based test setup.

3.2.2 Credence Tester and FPGA DUT Interface

A second Credence-based test architecture uses the Credence tester to send high-level commands to a field-programmable-gate-array (FPGA) board that manages all the details of running the DUT I/O. The Credence controls the retention time and load pattern for testing, and simplifies the test interface. As the Credence is only viable to send data at clock rates up to 50 MHz, all the high-speed I/O to the DUT would be controlled by the FPGA board.

While this option reduces the risk of limited expensive test boards that can be easily damaged, it uses the Credence tester. The Credence is a limited, physically unmovable resource. Its use for this testing cannot be combined with or run in parallel with other tests. As a result, it may be unavailable for long periods of time when it is not dedicated to the SDRAM test task. This is not how the tester was intended to be used and is not optimal for its intended design. By contrast, a computer can generate similar signals with more flexibility at a lower cost.

Both Credence-based approaches allow only one DUT at a time to be run and tested. This has huge consequences as a full sweep of retention speed tests will take up to 24 hours per test part. The impact becomes more apparent as test points and DUTs are added to the test matrix. For example, testing three devices at 10 temperature values will take 2–3 weeks.

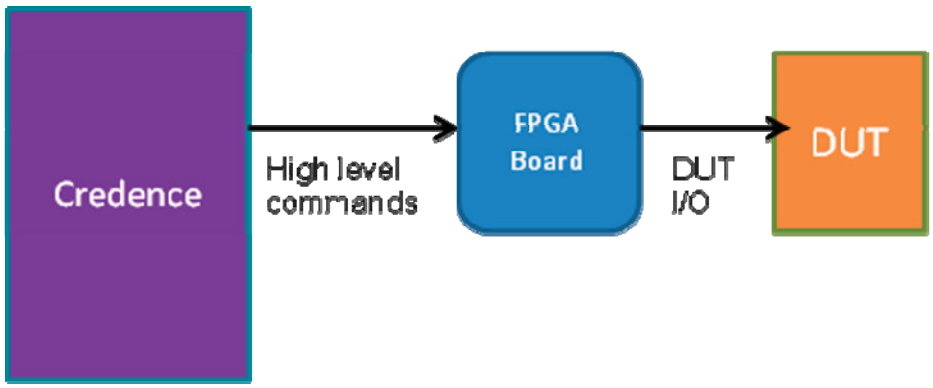


Figure 3.2-2. Credence and FPGA-based test setup.

3.2.3 Computer and FPGA Solution

The test setup selected forgoes using the Credence tester and, instead, uses a computer to control multiple stand-alone test setups that exercise a DUT.

This test system does not tie up any limited resources; therefore, it avoids any test bottleneck by running multiple tests in parallel. For example, by adding a second computer, another set of testers can be added and used in another physical location allowing for simultaneous measurements at different stress environments.

In addition to the increased resource availability of this set up, there are also technical advantages. The FPGA can customize and add clock-phase to allow for sampling at various intervals within the clock cycle. Scopes and logic analyzers in the laboratory can be used to verify the DDR2 at-speed operation. Finally, the robustness is increased by socketed parts on daughter cards and multiple test boards.

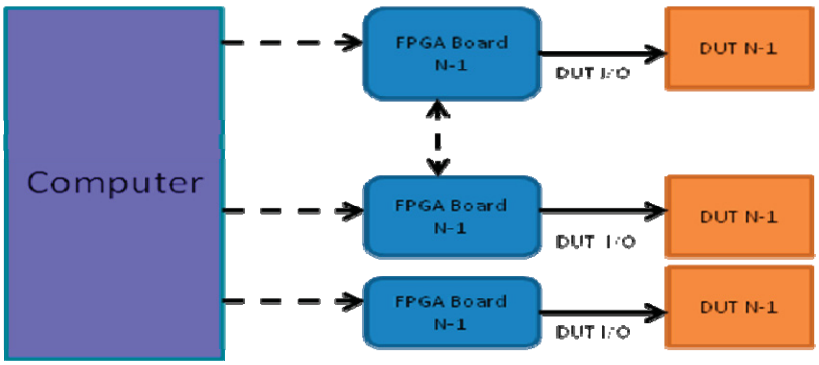


Figure 3.2-3. High-level concept tester approach. Not all intermediate hardware shown.

3.3 Tester Capabilities

The test system is designed with the ability to increase performance through further development of hardware and firmware. The current test system, used for the data presented in this paper, is capable of a frequency range of 25 to 125 MHz clock rate. The connector on the DUT daughter board should be functional from −200 to +250°C. This value depends on the mechanical stability of the board with changing temperatures. The refresh interval on the parts can vary from 64 ms until an arbitrarily long time period allowing for full retention time sweeps. The current actual data rate is 2 GB in approximately 100 seconds (20 Mb/second).

The next stage of test system development includes plans to increase its capabilities in data rate and increase the number of DUTs that can be tested on a single FPGA board.

3.4 Test System Architecture

The test system architecture consists of a laptop computer connected to an FPGA-based system consisting of four boards. Each of the four boards is inexpensive and can easily be exchanged for another adding a high degree of flexibility. The boards consist of a commercial USB interface board with a custom connector, a commercial FPGA evaluation board, a custom mezzanine card, and a DUT card with a mounted SDRAM device.

The computer uses a USB interface card from Opal Kelly to transfer data from the computer to multiple FPGA test boards. The data from the computer includes parameters and data for the test board to run a full test. This information is stored in the register files on the FPGA. In addition to the register files, the FPGAs contain finite state machines, which are capable of exercising the DUT without further input once parameters are set.

The DUT is connected to the FPGA board through a mezzanine card that connects to the FPGA board and attaches to the DUT board through a high-speed socket. The high-speed socket on the DUT card has signals that are compatible with the Goddard Space Flight Center (GSFC) low-cost digital tester's (LCDT's) socket 9.

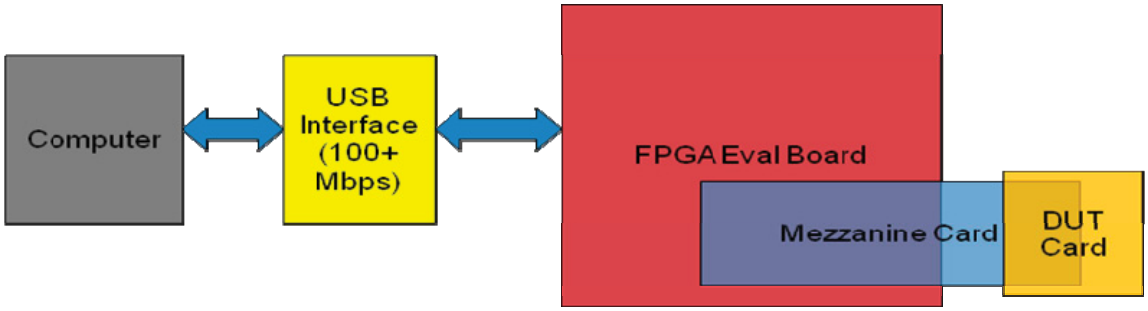


Figure 3.4-1. Overall system structure.

3.5 Board Designs

3.5.1 USB Interface

A USB interface was selected as the way to control the test hardware using the Visual Basic interface on the test computer. The interface card selected supports full USB2 (480 mbps) and provides a robust high-speed I/O interface to the FPGA evaluation boards.

The USB-to-FPGA connection is made through a hardware interface used to support a low-level transfer protocol. The hardware interface consists of eight input and eight output data signals along with control and status signals, referred to as the IO16 interface. The hardware interface is designed to run at 16 MHz. The interface enables a transfer protocol consisting of a combined address, data, and control (ADC) bus referred to as IO16_ADC (i.e., IO16_ADC is an abstract protocol supported by the IO16 hardware interface).

The IO16_ADC bus consists of the four simple buses described below:

ADDR:	32-bit address bus
DOUT:	32-bit data bus from the slave to the client application
DIN:	32-bit data bus from the client application to the slave
CTRL:	3-bit control signal bus

The ADC is used to write directly to the register file stored on the FPGA and can be used to set parameters, send data, control addressing, etc. The register file is then used by the FPGA's finite-state machines (FSMs) to determine how the DUT is exercised.

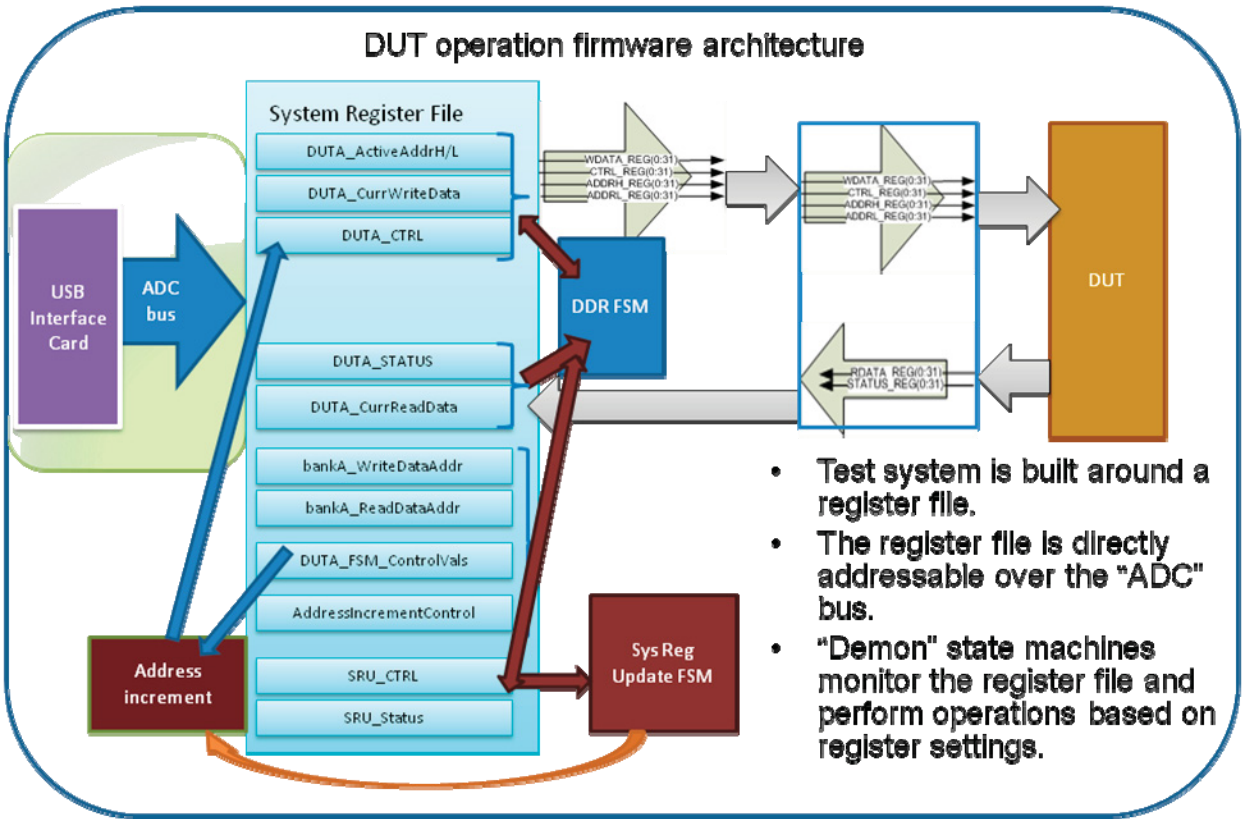


Figure 3.5-1. DUT operation firmware architecture with USB interface and ADC bus in upper left.

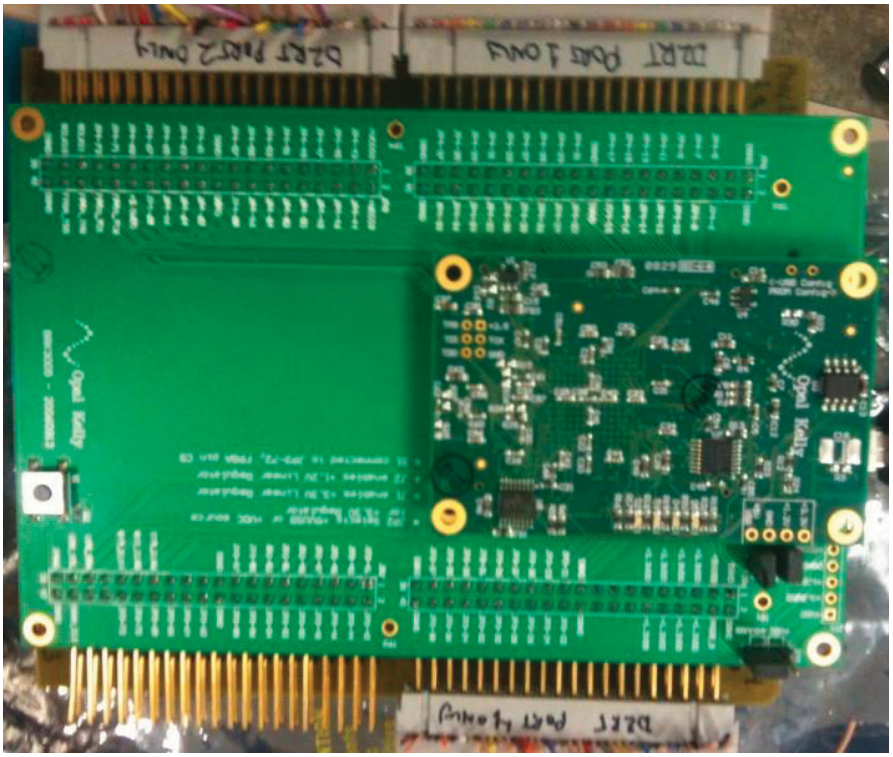


Figure 3.5-2. USB interface card in lab with multipe IO16 interfaces running to FPGA evaluation boards.

3.5.2 FPGA Evaluation Board

The FPGA boards control the high-speed I/O to and from the DUT through a DDR finite state machine. The parameters that control the DDR state machine are set in the system register file that resides on the FPGA. The parameters for the test are initially set by the ADC bus coming from the computer. Once a test begins, other FSMs within the FPGA update the address locations and registers to reflect the state of the test.

The FPGA evaluation boards used for the test were selected for their high-speed connectors and matched trace length. The high-speed connectors provide strong signal integrity to the FPGA and connected boards while the matched trace length decreases the probability of timing errors. The connectors support the number of signals necessary to exercise multiple DUT cards as the test setup grows. In addition to the high-speed connectors, the boards have additional ports that receive the ADC bus over the IO16 interface from the USB interface card.

The boards contain a Virtex-4 FPGA, which is powerful enough to run the tester design and any firmware upgrades as future test capabilities increases. The boards are available in high numbers at a fairly low cost allowing the purchase of 12 for under $10k.

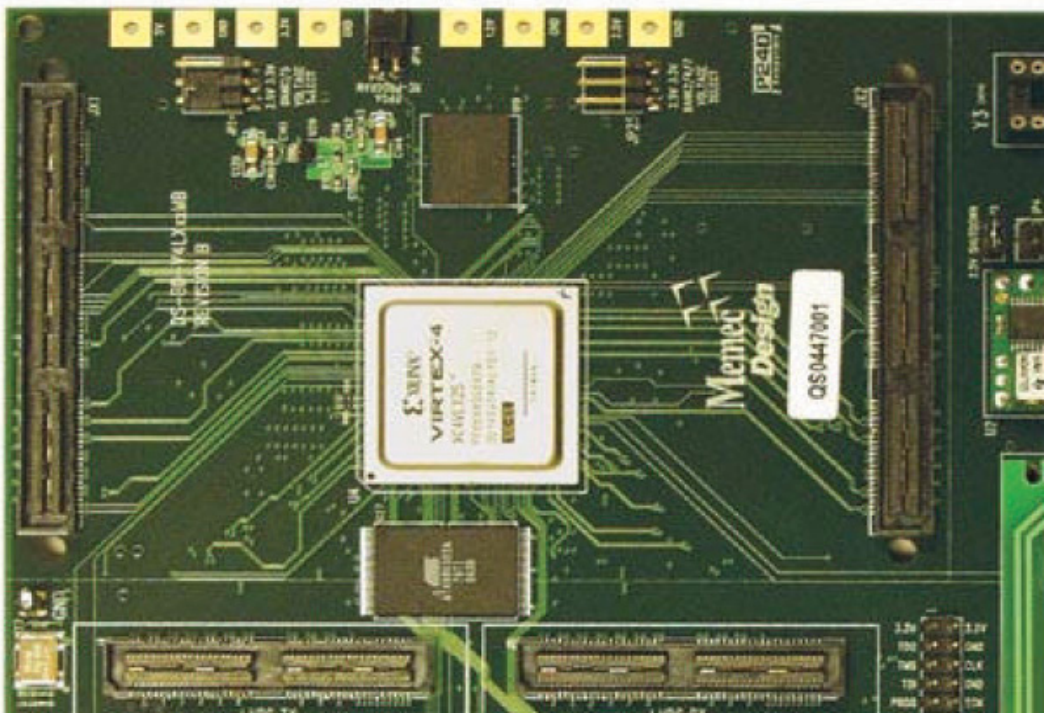


Figure 3.5-3. The FPGA evaluation board, DS-KIT-V4LX60MB-G (Avnet).

3.5.3 *Mezzanine Card*

Mezzanine cards provide a connection to the DUT cards with mounted parts and to the FPGA boards. The main purpose for the card is to provide a high-speed interface to LCDT compatible connectors on the DUT from the commercial FPGA board while providing environmental isolation on the DUT. Environmental isolation is achieved by mounting a mezzanine card between the doors of environmental chambers so that the DUT can be exposed to stress environments while the FPGA board is in a room-temperature, non-stressed environment. The mezzanine boards also provide custom capability on the FPGA evaluation board as the FPGA Vref signal (not the DUT Vref) is created on this board. By adding capability to the mezzanine card, it allows for simplified and smaller DUT cards allowing the isolation of DUT reliability issues from test system reliability issues.

The mezzanine board comes in two versions; the A version can connect to only one DUT card and has a separate support device that can be used to store values from the DUTs and the B version has multiple high-speed connectors, which can be used to run up to eight DUTs through one mezzanine card connected to one FPGA board.

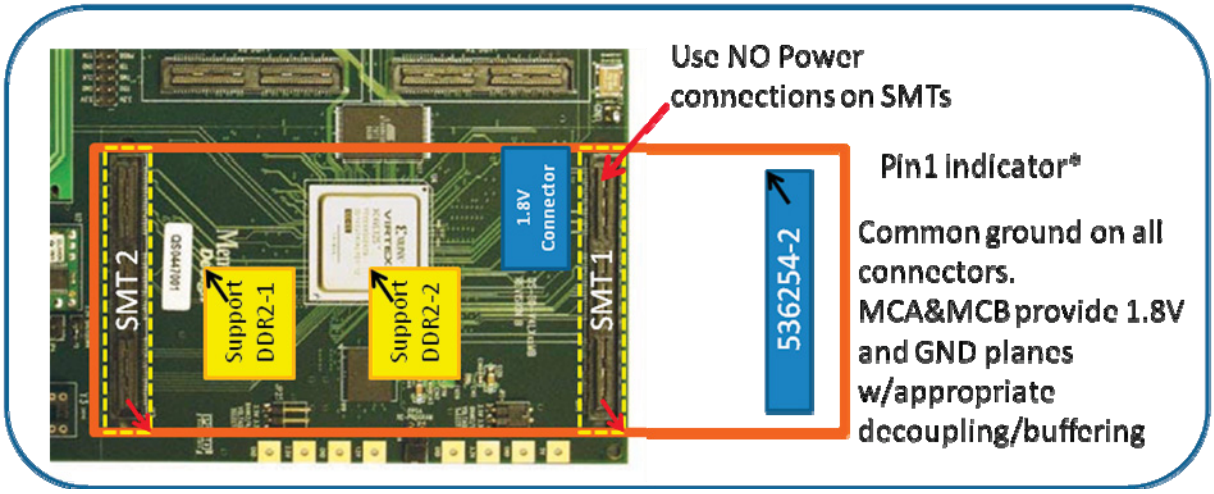


Figure 3.5-4. Diagram showing the connection of the mezzanine card to the FPGA board.

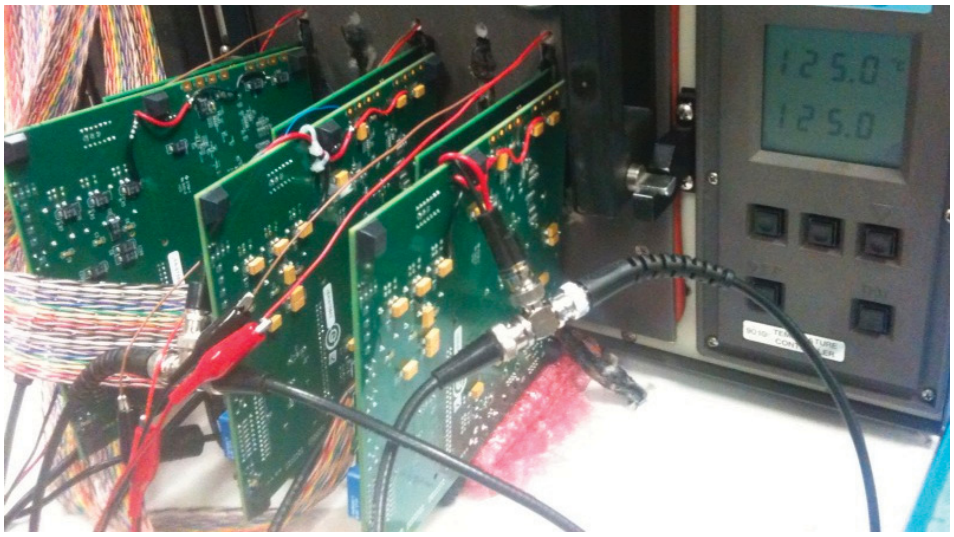


Figure 3.5-5. The mezzanine card as a physical interface between test environments.

Figure 3.5-6. The mezzanine card is shown connected to the DUT card and FPGA board.

3.5.4 DUT Card

The DUT daughter cards consist of a soldered DDR2 SDRAM device, a high-speed connector, and a power input for the DUT. These boards connect to the mezzanine cards and are intended to be placed inside the environmental chambers. The boards were kept as simple and robust as possible to keep the DUT reliability data uncontaminated by reliability issues in the DUT daughter card.

The DUT board was designed for compatibility with multiple part types and testers. Either a 60- or 68-pin fine ball grid array (FBGA) packaged part can be mounted to the DUT card, supporting x4 and x8 devices. It has an isolated power with a power connection so that the DUTs can be run at varying power levels with local generation of Vref. The signals on the socket are designed to be compatible with GSFC's LCDT socket 9.

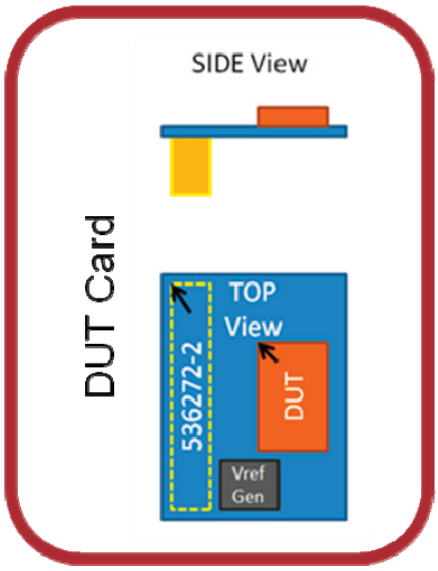


Figure 3.5-7. High-level schematic of the DUT card.

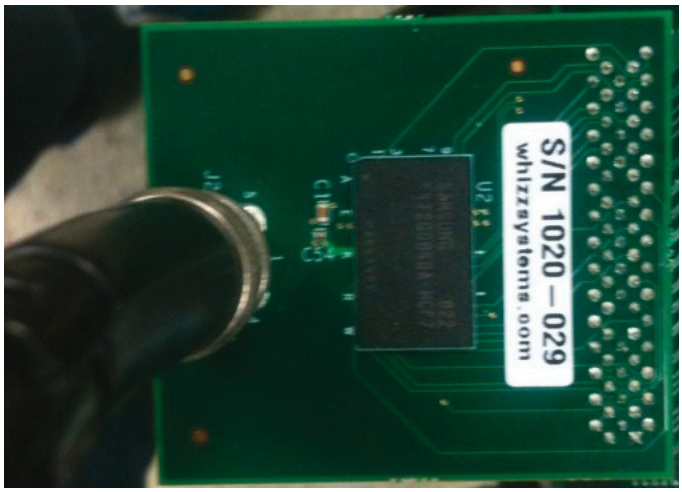


Figure 3.5-8. Picture of the DUT card with Samsung DDR2 mounted.

3.6 Test Setup

The tests on the DDR parts consist of stressing the parts by stimulating them with continuous read/write operations at either 1.8 V or 2.7 V while the temperature is held at a constant value (−5°C , 25°C, or 125°C). The setup to achieve these levels is described below.

3.6.1 Nominal Voltage Setup

Characterization of the DUTs between tests is performed at the nominal voltage value of 1.8 V. To run at this level, it is important that the FPGA is programmed using the firmware version specified for that voltage. After programming the FPGA, the voltage levels for the mezzanine board and the DUT card can then be set to 1.8 V.

3.6.2 Voltage Stress Setup

To induce voltage stress, the parts are run at 2.7 V. In order to achieve 2.7 V (1.5 × Vdd) operation, the test system configures the DUTs with 2.5 V Stub Series Terminated Logic (SSTL) compatible signals, then runs at the high side of the specification [2], delivering 2.7 V. To do this, the FPGA needs to be programmed with the firmware version that is specified for 2.7 V. After it has been programmed, the DUT and mezzanine card can ramp up their voltage, in parallel, to 2.7 V.

3.6.3 Temperature Stress Setup

Tests performed at temperatures other than room temperature, such as specification maximum and thermal stress levels, are performed with the DUT running inside a thermal chamber. The mezzanine board runs between the chamber door with its DUT card connection inside the chamber to expose the DUT to the temperature environments. On the other side of the mezzanine board, the FPGA, USB interface card, and computer are all external and operating at room temperature. The chamber and modified door are capable of accommodating three mezzanine boards and simultaneously exercising three DUTs. The 25°C, or room temperature, test uses the same electrical interfaces, but the mezzanine board is not used as a physical bridge into an environmental chamber.

4.0 TESTS CONDUCTED

4.1 Stress Test Matrix

The parts are divided into sets of three and subjected to continued stress while continuously being exercised. Before and after being stressed, the parts are placed in nominal operating conditions and their performance is characterized through a series of experiments, including current measurements and retention sweeps.

Table 4.1-1 lists the types of continuous stress to which the parts are subjected. This table has a row for each of the tested set of DUTs and specifies the temperature and voltage level at which each set was stressed.

In fiscal year 2011, the matrix will be expanded, populated with additional measurements of both the Samsung and Micron parts. The decision for what tests correspond to each set of parts will depend on the results of preliminary data.

The −55°C and 125°C tests are conducted, as described in Section 3.6, using a thermal chamber with a door modified to allow mezzanine boards to go through insulated slots from outside the chamber to inside.

During stress, the parts are run at either the nominal 1.8 V or at 2.7 V to induce voltage stress.

Table 4.1-1. Part Stress Test Matrix

Stress	Temperature			Voltage		Stress Hours
	−55°C	25°C	125°C	1.8 V	2.7 V (1.5 x Vdd)	
Samsung (set 1)			X		X	245
Samsung (set 2)		X			X	0 (Pre-stress only)

4.2 Stress Test and Characterization Overview

At various intervals, the parts are returned to in-specification values and tested through a series of experiments to determine the impact of the stress:

- Experiment 1—Retention time sweep at room temperature. This test helps determine the impact of long-term previous stress on the relationship between data loss and increased refresh rate.
- Experiment 2—Retention time sweep at maximum specification temperature (75°C/85°C—some data was taken with 75°C as the high temperature, but the specification maximum is actually 85°C, and in the case of Samsung it is dependent on refresh rate). This test explores the relationship between in-specification temperature stress and long-term stress on the relationship between data loss and refresh rate.
- Experiment 3—Measure Read/Write/Standby current. Increased current reflects increased leakage through points within the complex array of internal circuitry [1].

These experiments were selected because previous data indicated that the following parameters were most changed by stress conditions [1]:

- Operating current
- Auto refresh current
- Data retention time (Tret)

The retention time sweep tests are the most time consuming and consist of continually doubling the retention time on devices to chart the data lost at each retention time (refresh rate). According to the manufacturers specification, the devices must be refreshed every 64 milliseconds, after this point, the data can degrade and information is lost. The weakest bits generally lose data shortly after 64 milliseconds at specification maximum temperature, but other bits may retain their data for hours or even days.

4.3 Part Characterization Test Flow and Procedures

The steps used to perform the characterization of the parts before and after the parts are stressed are outlined below.

All devices are baselined through a characterization test before being subjected to stress conditions. This verifies part functionality before stress and provides a functional data point for comparison. The following areas cover the procedures followed to run the pre-stress and post-stress characterization test and the continuous part stress.

4.3.1 Pre/Post-Stress Characterization

The characterization test is intended to measure the following parameters on each of the devices and to see how those values shift as a result of time exposed to the stress conditions.

1. Standby current
2. Current during writing to the array
3. Current during reading from the array
4. Number of bits (or fraction of all bits) that lose their data based on the refresh interval

The three experiments mentioned in Section 4.2 are completed by performing the characterization at both the room temperature (experiment 1) and the maximum temperature indicated on the part specification (experiment 2). During both of these tests, the current during read, write, and standby is monitored and recorded, satisfying experiment 3.

4.3.2 Characterization Test Procedure

The steps for running a characterization test are as follows:

1. Place DUT card with DUT being characterized in socket of mezzanine card of test system used for characterization. The test system will either be on a table top at room temperature or will use a thermal chamber to heat the DUT to the maximum specification temperature.
2. Power on test system to nominal voltage levels.
3. Use the Visual C++ interface program to communicate with the device and enter retention sweep menu.
4. Before beginning retention sweep, note the standby current of the device.
5. Begin retention sweep and record the write current.
6. After a few minutes after starting the retention sweep, the Visual C++ software system indicates that it is in read mode. During this time, record the read current.
7. The retention sweep will continue for several hours outputting results into a log file. Once the test is complete, the number of bit errors with each retention time is recorded. Store this file with information on current values to have a full characterization record.

4.3.3 Pre-Stress Baseline Measurements

Before using a test device, it is pre-characterized to determine its initial retention sweep curve and baseline current (which may be different than the specification values) as well as to verify standard functional behavior.

The initial characterization includes the additional step of verification of the test setup and DUT. This is done by running a write and read cycle and verifying that more than 50% of the data bits have no errors (i.e., at least four of the eight data pins have no errors). This helps to determine that the part has no damage and verifies that the test system is working. Some data lines on the mezzanine card may have timing problems on bit lines due to different trace-lengths and differences in connection quality through the connectors.

In addition to verifying test setup functionality, a pre-stress test is important to get baselined current values as they may be inconsistent with the specification values listed in Appendix B. When comparing the specification values for current to the measured values, it is important to note the following factors that may result in values inconsistent with the specifications.

1. The measured current depends on the operating frequency of the device. The higher the frequency, the higher the current.
2. The test devices operate with a clock rate of 125 MHz while the operational current is usually specified for 400 MHz or higher.
3. In the case of active standby current, the test board does not deassert CS\. As a result, the reported “standby” currents are similar to the specification’s active standby current but not identical (in addition to not meeting the frequency).

As this test is concerned with changes in performance as a result of environmental stress, it is more important to understand how a current changes from baseline rather than how it compares to the values in the spec sheet.

4.3.4 DUT Operation under Stress

In order to examine reliability mechanisms in the cells of the DDR2 devices, it is necessary to apply stress fields within the data storage elements. This is the reason the DUTs must be operated during stress. By operating the DUTs in a refresh mode during elevated voltage and temperature, the DUT cells will hold higher internal electric fields, which are required for activating failure mechanisms.

The DUTs are fully operated under stress, by performing read and write operations fast enough to ensure meeting the 64 ms refresh requirement. The entire DUT address space is sampled. The pattern used to program the cells is address-based, ensuring exactly 50% of the bits are ‘0’s and 50% are ‘1’s. By performing these operations on the DUT under stress, we ensure that pattern dependence is sampled roughly, and that the entire device must be working in order to get the test setup to pass requirements for data taking.

As stated before, some bit lines on the DUT are not reliable for detailed testing due to connection and timing issues (special timing files for each DUT introduce too much risk to the entire test matrix and were rejected). All DUTs are required to have at least four bit lines with no problems (no errors) in order for a DUT to be considered viable for testing.

Stress testing calls for 2.7 V operation of DUTs. This is out of specification, and thus the operation of the DUT cannot be tested in a normal way at this voltage. It was inferred that DUT

operation was nominal during elevated voltage stress by the following observations. The currents changed in similar ways at 2.7 V during operation as they did at 1.8 V during operation. Many of the bit lines actually operate nominally at 2.7 V (this is not at all predictable because the Vref is completely out of specification, and the DUT is expected to be internally regulating power, this means the detection of logic high and logic low may be significantly altered). Finally, the 2.7 V operation is considered nominal if it is also shown that upon returning to 1.8 volts the DUT operation returns to (potentially degraded) earlier observed operating conditions.

5.0 PRELIMINARY TEST RESULTS

5.1 Test Devices

At this point, only the Samsung parts have characterization data. One set of three parts has pre- and post-stress data and has been subjected to active dynamic stress testing while exposed to 125°C. Another set of three parts has pre-stress characterization data and will be used for 25°C, 2.7V stress testing.

5.1.1 Pre-Stress Retention Sweeps

Data from the pre-stress retention sweeps for the first three test parts are shown in Figures 5.1-1 (room temperature) and 5.1-2 (75°C).

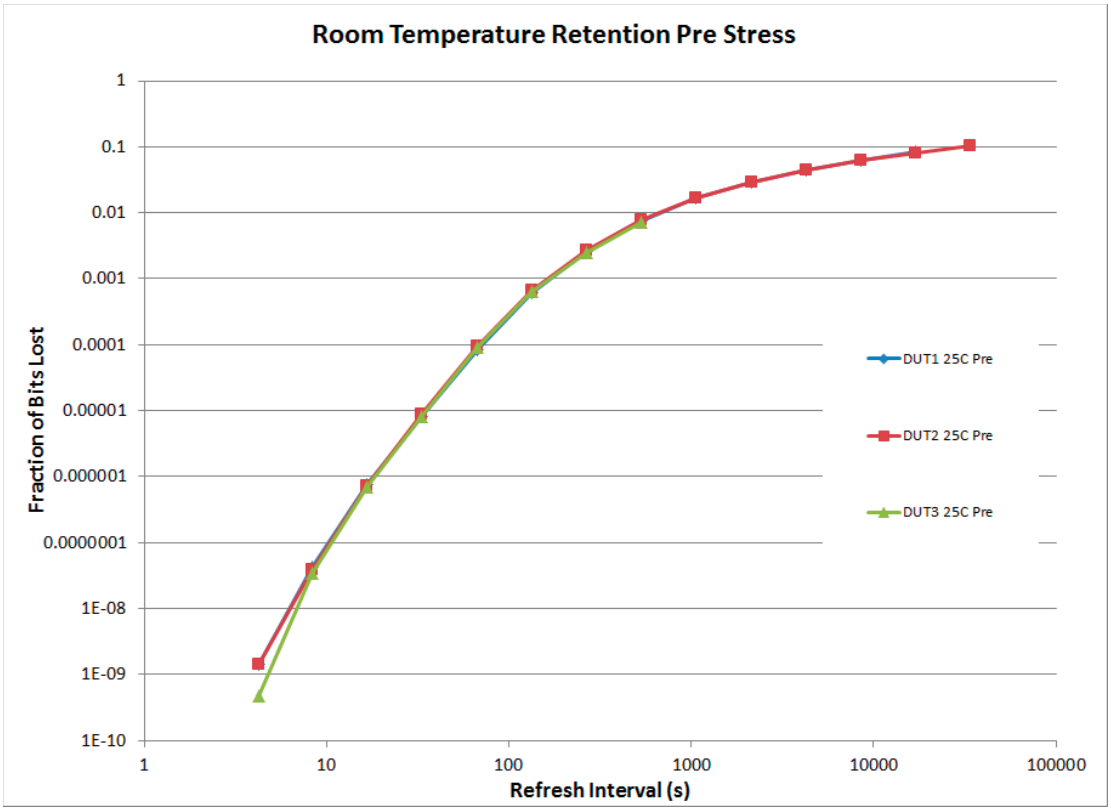


Figure 5.1-1. Pre-stress room temperature retention characterization of the 125°C DUT set.

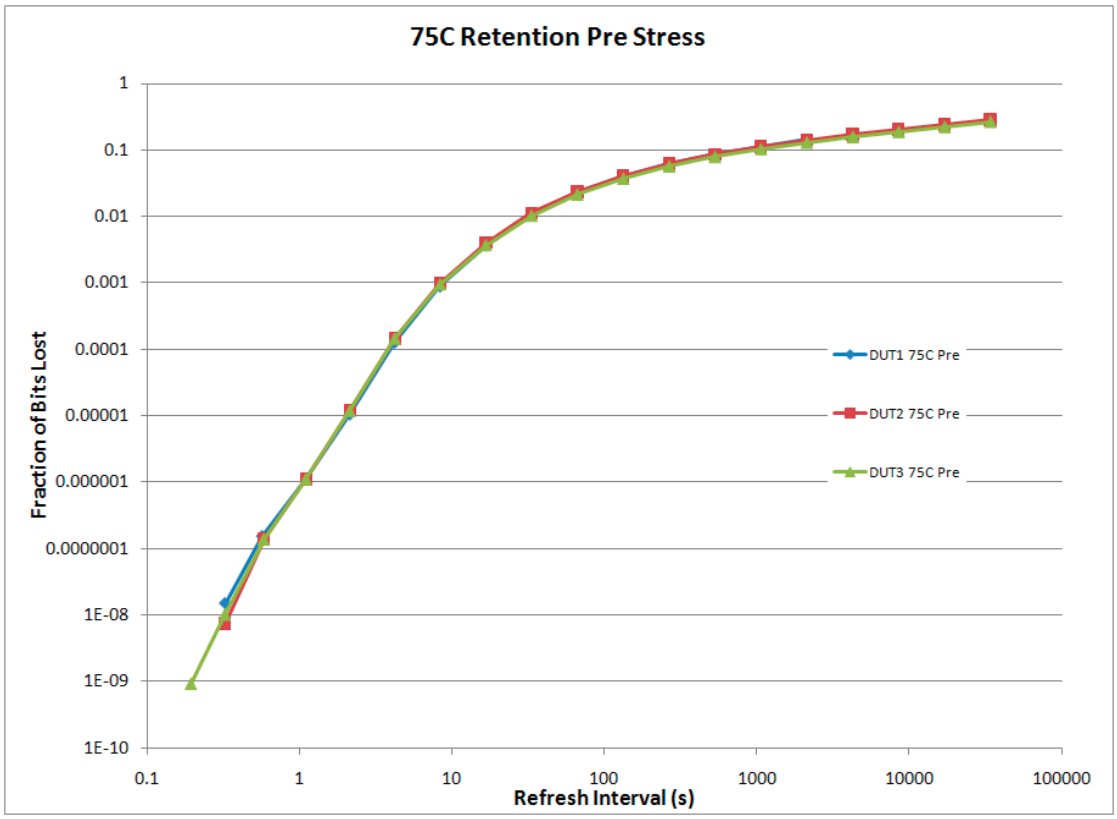


Figure 5.1-2. Pre-stress 75°C retention characterization of the 125°C DUT set.

5.2 Stress Study

5.2.1 Current vs. Tstress

Only the first set of DUTs have received a significant amount of stress hours. As of this report, significant changes to the current values have started and are expected to increase with stress hours. This report only shows the 0 and 250-hour stress points. The measurements at pre-stress and at 250 hours of 125°C stress and 2.7 V are shown below in Table 5.2-1.

Table 5.2-1. The observed IDDQ values across three test parts stressed at 125°C.

DUT	IDDQ	Value (25°C), No Stress	Value (25°C), 250-Hrs Stress	Value (75°C), No Stress	Value (75°C) 250-Hrs Stress
1	IDD3N*	21.9 mA	21.9	20.9	21.2
1	IDD4W*	24.9	24.8	21.3	N/A
1	IDD4R*	24.8	24.9	19.8	N/A
2	IDD3N*	21.7	21.7	21.3	21.5
2	IDD4W*	24.7	24.8	23.7	24
2	IDD4R*	24.7	24.7	23.6	N/A
3	IDD3N*	21.9	19.8	19.8	19.5
3	IDD4W*	23.9	23.1	22.4	22.4
3	IDD4R*	23.8	N/A	22.4	22.4

* These tests require 400 MHz for the specification, but testing was performed at 125°C. Also, for IDD3N, CS\ is supposed to be high, but here it is held low.

5.2.2 *Retention Sweeps*

The retention curves were analyzed for changes over the limited stress exposure. Figures 5.2-1 and 5.2-2 show the curves for the three DUTs exposed to 125°C. The pre-stress curves and post-250-hour curves are plotted on the same figure.

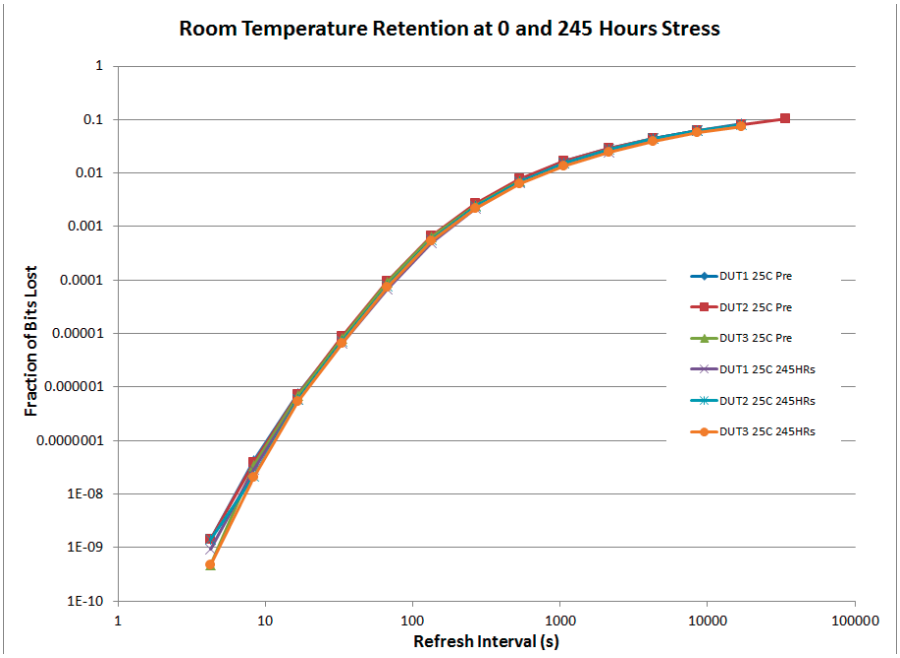


Figure 5.2-1. The retention curves at room temperature (25°C) for the 0 and 245-hour stress points on DUT set 1 (where stress is 2.7 V and 125°C).

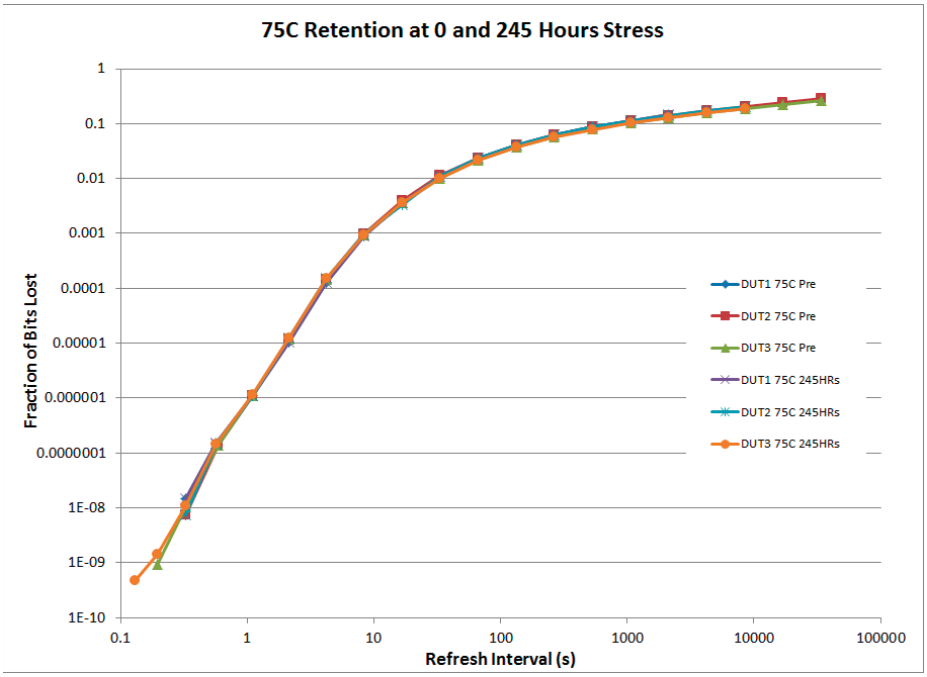


Figure 5.2-2. The retention curves at 75°C for the 0 and 245-hour stress points on DUT set 1 (where stress is 2.7 V and 125°C).

5.3 Discussion

Thus far, no significant changes have been observed in the retention curves. Based on trends in previous year's work [1], changes are expected to appear as stress hours exceed the 500-hour point. At this point, there is an approximately 5% increase in the current measurements, indicating damaging modifications to circuit structures have created increased leakage. These indicate that significant device impact is expected to begin manifesting.

In addition, although the plots look very similar, it is possible that the log-log nature of the presentation (required for data covering so many orders of magnitude) is obscuring key information. The control experiment for the temperature stress is presently about to hit 250 hours. When that happens, it may be possible to see if the increased spread in the comparison of the retention curves is due to natural variation in device response, or if it is due to stress-related effects.

Whether the voltage stress tests will yield significant results is debatable as it is believed that internal regulation lowers the 2.7 V external voltage internally back to 1.8 V. If true, the Vdd stress values are not applied to the memory cores. A possible interesting result of the impact of Vdd stress is that it may trigger other failure modes from the increased power dissipation and Vref pins being too high for internal regulation compromising data integrity and operational reliability.

6.0 FUTURE WORK

6.1 Updated Tester

Boards have been developed and procured to expand the test capabilities to allow multiple DUTs to run on one FPGA board. The mezzanine card B (MCB) has connectors to attach up to eight DUTs with current plans expecting the use of three DUTs per board. To use these boards, further firmware and test setup development is required. Since each socket requires custom tuning, initial efforts will target only three sockets.

Figure 6.1-1 shows an early design for MCB with the general structure. It has since been modified from nine down to eight DUT sockets.

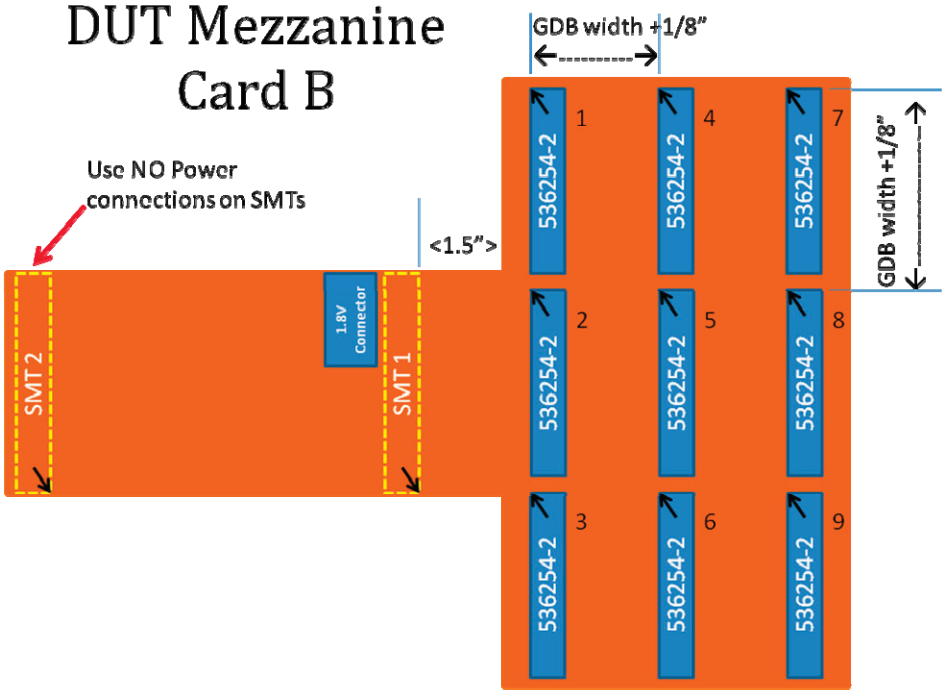


Figure 6.1-1. Mezzanine card B used to control multiple DUTs through a single FPGA board.

6.2 Proton Testing

Proton exposure will be added to future tests to provide more space-like environment models for reliability and examine synergy between displacement damage dose (DDD) and cell retention and part reliability. Previous testing on DDR2 SDRAMs indicated that after exposure to protons, the weakest cells in a part begin to reduce their retention time. A combined temperature and proton test could provide data that will increase understanding of the radiation/reliability relationship. This understanding could lead to a standard model for analyzing the combined impact of radiation and reliability factors to part parameters.

The appropriateness of protons versus other types of radiation exposure (such as total ionizing dose [TID]) was analyzed. Published documents show that TID leads to a broad shift of all cells while not making any bits significantly weaker than the others [3]. Protons and heavy ions, on the other hand, lead to several orders of magnitude shifts in the retention time of the cells that are the most directly impacted.

6.3 −55°C Tests

The test setup for running the DUTs at −55°C has been developed and data will be collected and reported in the future. The setup is similar to the 125°C test setup with a more robust and insulated chamber door for mounting and inserting the mezzanine card through to avoid condensation and electrical failures. The goal of the low temperature tests is to identify the increased leakage of the dielectric of the storage capacitors by charge injection under stress before breakdown of the dielectric. This was an effect explored through low temperature testing in the previous work on DDR1 SDRAM [1].

7.0 REFERENCES

[1] White, M., *Scaled CMOS Technology Reliability Users Guide*. JPL Pub 09-33. Available at: http://trs-new.jpl.nasa.gov/dspace/bitstream/2014/41491/1/JPLPUB09-33.pdf

[2] Xilinx, "Virtex-4 FPGA Data Sheet: DC and Switching Characteristics," 2009.

[3] Scheick, L. Z., Guertin, S. M., and Swift, G. M.. "Analysis of Radiation Effects on Individual DRAM Cells" *IEEE Trans. Nuclear Sci,* Vol. 47, No 6, pp. 2534–2538, 2000.

[4] Samsung, Samsung K4T2G084QA-HCF7 Data Sheet, Rev.1.3, 2008.

[5] Micron, Micron MT47H256M8HG-3:A Data Sheet, Rev. D, 2010.

APPENDIX A. ACRONYMS AND ABBREVIATIONS

ADC	address, data, and control
CMOS	complementary metal oxide semiconductor
DDD	displacement damage dose
DQ	data line where Q is 0-7
DUT	device under test
FBGA	fine ball grid array
FPGA	field programmable gate array
FSM	finite-state machine
GSFC	Goddard Space Flight Center
IDD	total device current
IDD(q)	Idd drawn by device while in operating mode q.
I/O	input/output
JPL	Jet Propulsion Laboratory
LCDT	low-cost digital tester
MCB	mezzanine card B
MCA	mezzanine card A
NEPP	NASA Electronic Parts and Packaging
SSTL	Stub Series Terminated Logic
TID	total ionizing dose
TBC	to be confirmed
TBD	to be determined

APPENDIX B. PART DATA SHEET VALUES

Part Specifications for the DDR2 SDRAM devices tested.

Samsung K4T2G084QA-HCF7 Data Sheet Information

Table B-1. Samsung DDR2 SDRAM IDD specification parameters and test conditions [4].

Symbol	Proposed Conditions		Units	Notes
IDD0	**Operating one bank active-precharge current**; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RC = {}^{t}RC(IDD)$, $^{t}RAS = {}^{t}RASmin(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RC = {}^{t}RC$ (IDD), $^{t}RAS = {}^{t}RASmin(IDD)$, $^{t}RCD = {}^{t}RCD(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address businputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current**; All banks idle; $^{t}CK = {}^{t}CK(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; $^{t}CK = {}^{t}CK(IDD)$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputsare STABLE; Data bus inputs are FLOATING		mA	
IDD2N	**Precharge standby current**; All banks idle; $^{t}CK = {}^{t}CK(IDD)$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD3P	**Active power-down current**; All banks open; $^{t}CK = {}^{t}CK(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	mA	
		Slow PDN Exit MRS(12) = 1	mA	
IDD3N	**Active standby current**; All banks open; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RAS = {}^{t}RASmax(IDD)$, $^{t}RP = {}^{t}RP(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RAS = {}^{t}RASmax(IDD)$, $^{t}RP = {}^{t}RP(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RAS = {}^{t}RASmax(IDD)$, $^{t}RP = {}^{t}RP(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD5B	**Burst auto refresh current**; $^{t}CK = {}^{t}CK(IDD)$; Refresh command at every $^{t}RFC(IDD)$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD6	**Self refresh current**; CK and CK\ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA	
		Low Power	mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $^{t}RCD(IDD)-1*{}^{t}CK(IDD)$; $^{t}CK = {}^{t}CK(IDD)$, $^{t}RC = {}^{t}RC(IDD)$, $^{t}RRD = {}^{t}RRD(IDD)$, $^{t}FAW = {}^{t}FAW(IDD)$, $^{t}RCD = 1*{}^{t}CK(IDD)$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		mA	

Table B-2. Samsung DDR2 SDRAM IDD specifications table [4].

Symbol	256Mx8 (K4T2G084QA)						Unit	Notes
	800@CL=5		800@CL=6		667@CL=5			
	CE7	LE7	CF7	LF7	CE6	LE6		
IDD0	95		95		90		mA	
IDD1	120		120		110		mA	
IDD2P	15	8	15	8	15	8	mA	
IDD2Q	55		55		50		mA	
IDD2N	60		60		55		mA	
IDD3P-F	50		50		40		mA	
IDD3P-S	18		18		18		mA	
IDD3N	80		80		70		mA	
IDD4W	170		170		150		mA	
IDD4R	200		200		170		mA	
IDD5	280		280		260		mA	
IDD6	15	8	15	8	15	8	mA	
IDD7	350		350		320		mA	

Table B-3. IDD values in the Samsung DDR2 characterized before and after stress [4].

IDD3N	**Active standby current** All banks open ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; other control and address bus inputs are SWITCHING; data bus inputs are SWITCHING	mA
IDD4W	**Operating burst write current** All banks open; continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; address bus inputs are SWITCHING; data bus inputs are SWITCHING	mA
IDD4R	**Operating burst read current** All banks open; continuous burst reads; IOUT – 0 mA; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; address bus inputs are SWITCHING; data patter is same as IDD4W	mA

Table B-4. Samsung DDR2 SDRAM absolute maximum DC ratings [4].

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	- 1.0 V ~ 2.3 V	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Table B-5. Samsung DDR2 SDRAM recommended DC operating conditions [4].

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1,2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

Table B-6. Samsung DDR2 operating temperature condition [4].

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating Temperature	0 to 95	°C	1, 2

Table B-7. Micron DDR2 SDRAM absolute maximum DC ratings [5].

Parameter	Symbol	Min	Max	Units
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–1.0	2.3	V
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.5	2.3	V
V_{DDL} supply voltage relative to V_{SSL}	V_{DDL}	–0.5	2.3	V
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	2.3	V
Input leakage current; any input 0V ≤ V_{IN} ≤ V_{DD}; all other balls not under test = 0V)	I_I	–5	5	µA
Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT disabled	I_{OZ}	–5	5	µA
V_{REF} leakage current; V_{REF} = valid V_{REF} level	I_{VREF}	–2	2	µA

Table B-8. Micron DDR2 SDRAM temperature limits [5].

Parameter	Symbol	Min	Max	Units
Storage temperature	T_{STG}	–55	150	°C
Operating temperature – commercial	T_C	0	85	°C
Operating temperature – industrial	T_C	–40	95	°C
	T_{AMB}	–40	85	°C

Table B-9. Micron DDR2 SDRAM general IDD parameters [5].

I_{DD} Parameters	-187E	-25E	-25	-3E	-3	-37E	-5E	Units
CL (I_{DD})	7	5	6	4	5	4	3	^tCK
^tRCD (I_{DD})	13.125	12.5	15	12	15	15	15	ns
^tRC (I_{DD})	58.125	57.5	60	57	60	60	55	ns
^tRRD (I_{DD}) - x4/x8 (1KB)	7.5	7.5	7.5	7.5	7.5	7.5	7.5	ns
^tRRD (I_{DD}) - x16 (2KB)	10	10	10	10	10	10	10	ns
^tCK (I_{DD})	1.875	2.5	2.5	3	3	3.75	5	ns
^tRAS MIN (I_{DD})	45	45	45	45	45	45	40	ns
^tRAS MAX (I_{DD})	70,000	70,000	70,000	70,000	70,000	70,000	70,000	ns
^tRP (I_{DD})	13.125	12.5	15	12	15	15	15	ns
^tRFC (I_{DD} - 256Mb)	75	75	75	75	75	75	75	ns
^tRFC (I_{DD} - 512Mb)	105	105	105	105	105	105	105	ns
^tRFC (I_{DD} - 1Gb)	127.5	127.5	127.5	127.5	127.5	127.5	127.5	ns
^tRFC (I_{DD} - 2Gb)	195	195	195	195	195	195	195	ns
^tFAW (I_{DD}) - x4/x8 (1KB)	Defined by pattern in Table 9 (page 28)							ns
^tFAW (I_{DD}) - x16 (2KB)	Defined by pattern in Table 9 (page 28)							ns

Table B-10. DDR2 IDD specifications and conditions [5].

Parameter/Condition	Symbol	Configuration	-25	-3E/-3	-37E	-5E	Units
Operating one bank active-precharge current: $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD0}	x4, x8	115	100	90	90	mA
		x16	150	135	115	115	
Operating one bank active-read-precharge current: Iout = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MIN (I_{DD}), $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}	I_{DD1}	x4, x8	165	145	105	105	mA
		x16	180	160	135	135	
Precharge power-down current: All banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2P}	x4, x8, x16	12	12	12	12	mA
Precharge quiet standby current: All banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2Q}	x4, x8	65	55	45	40	mA
		x16	75	65	45	40	
Precharge standby current: All banks idle; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD2N}	x4, x8	70	60	50	45	mA
		x16	80	70	60	50	
Active power-down current: All banks open; $^{t}CK = {}^{t}CK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD3Pf}	Fast PDN exit MR[12] = 0	45	40	35	30	mA
	I_{DD3Ps}	Slow PDN exit MR[12] = 1	14	14	14	14	
Active standby current: All banks open; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD3N}	x4, x8	65	55	45	40	mA
		x16	85	75	55	50	
Operating burst write current: All banks open, continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4W}	x4, x8	180	160	130	125	mA
		x16	270	250	190	160	
Operating burst read current: All banks open, continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4R}	x4, x8	190	170	150	140	mA
		x16	295	275	195	180	

Table B-11. DDR2 IDD specifications and conditions (continued) [5].

Parameter/Condition	Symbol	Configuration	-25	-3E/-3	-37E	-5E	Units
Burst refresh current: $^{t}CK = {}^{t}CK$ (I_{DD}); refresh command at every ^{t}RFC (I_{DD}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD5}	x4, x8	300	280	260	250	mA
		x16	300	280	260	250	
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{DD6}	x4, x8, x16	12	12	12	12	mA
	I_{DD6L}		8	8	8	8	
Operating bank interleave read current: All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = ^{t}RCD (I_{DD}) - 1 x ^{t}CK (I_{DD}); $^{t}CK = {}^{t}CK$ (I_{DD}), $^{t}RC = {}^{t}RC$ (I_{DD}), $^{t}RRD = {}^{t}RRD$ (I_{DD}), $^{t}RCD = {}^{t}RCD$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching (see Table 9 (page 28) for details)	I_{DD7}	x4, x8	390	340	295	295	mA
		x16	445	395	355	355	